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... program was less efficient than **machine code** and required ... for the human user to **generate** a program ... Research in **artificial intelligence** has been primarily based ...
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Natural Language Processing

... We have the ability to **generate** sentences that are ... Research in AI (**Artificial Intelligence**) has been ... English (etc) <--- **machine code**; sign language <---> voice; ...
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Automatic Derivation of Code Generators from Machine Descriptions

... 25 REISER, J., ET AL. SAIL Stanford **Artificial Intelligence** Lab. Memo. ... 33 Wmcox, TR Generating **machine code** for high-level programming languages. ...
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Evolution of Complexity

... present our experiments in utilizing evolution to **generate** complexity in ... the dawn of the era of true **artificial intelligence**. ... Tierran genomes are **machine code**. ...
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Why Poplog Pop-11 was never implemented in C

... compiler which has to **generate** **machine code** for the ... However, instead of generating **machine code** directly from ... Science Volume 5: **Artificial Intelligence**, eds D ...
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Evolutionary and Adaptive Systems (EASy) at Sussex

... I argue that the use of **Artificial Intelligence** techniques such ... The **machine code** evolution system is found to ... be the starting point to **generate** cell boundaries ...
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CMU Artificial Intelligence Repository Home INFO Search FAQs ... library in order to **generate**

executables. ... translation of abstract **machine code** to corresponding C ...

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Manual, 1996. ... J. Russell, Peter Norvig, **Artificial intelligence**: a modern ...

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Olin Shivers MIT **Artificial Intelligence** Laboratory April 25, 1996 ... the macro-expanders

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... are needed for the generation of **machine code** because of ... of the field known as **artificial intelligence** (AI). ... scenes how to understand and **generate** speech or ...

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... computer programmer from the **Artificial Intelligence** Laboratory at ... tiny, self-replicating **machine code** programs, which ... and the ones that **generate** error messages ...

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... 4. The model can **generate** a new machine ... For various **artificial intelligence** models and neuron models, from the ... have three periods: the **machine code** period, the ...

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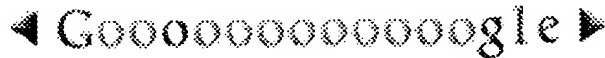
... Nets and Description Matching; **Generate** and test ... for the CS547 Graduate level **Artificial Intelligence** course taken ... Stack **machine code** tends to be smaller than a ...

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1 Introduction to Artificial Intelligence

... a machine understand and **generate** human language ... as they pertain to **Artificial Intelligence** operate at a ... the most thorough understanding of arcane **machine code**. ...

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... It can compile a C-- code to **generate MIPS machine code**. ... Communication, Compiler Design, Computer Graphics, **Artificial Intelligence**, Computer Architecture ...
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... called a compiler) converts the high level code to **machine code**. ... Scheme: good for
artificial intelligence. ... Dev C++ will automatically **generate** most of the code. ...
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... is added to the new **database** one by one ... called TrapDis- patcher into this low-memory

exception vector. ... the dispatch number following the TRAP **op- code**, and uses

...
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... an error such as an illegal **op-code**, it calls ... processor and that region belongs to the **database**. ... unique longword location in the **exception vector** table located ...

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... 154 6.2.3 User **Database**154

6.3 S ...

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... A-12 B The Design **Database**

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- 1 **Motorola 68040 microprocessor simulation for the Sun Workstation**
Trey Grubbs, Bill Herring, Richard Tan, Susan Mengel
April 1994 Proceedings of the 1994 ACM symposium on Applied computing
Full text available: pdf(769.14 KB) Additional Information: full citation, references, index terms

Keywords: computer aided instruction, microprocessr simulators

- 2 **A 16-bit microprocessor with multi-register bank architecture**
Hideo Maejima, Hiroyuki Kida, Tan Watanabe, Shiro Baba, Keiichi Kurakazu
November 1999 Proceedings of 1986 fall joint computer conference on Fall joint cc
Full text available: pdf(500.78 KB) Additional Information: full citation, references, index term

3 Just what is an op-code?: or a universal computer design

James Brakefield

June 1982

ACM SIGARCH Computer Architecture News, Volume 10 Issue 4

Full text available:  pdf(276.18 KB)

Additional Information: full citation, abstract

The following computer architecture offers extensible machine language. This does this by using the same format for both op-codes and subroutine calls. The programmer can choose an instruction set for the application at hand. I.e., the program can correspond to a high level textual representation or a program. This architecture is essentially a w ...

4 The internal machine

Andrew M. Welin

November 1973

Proceedings of the ACM-IEEE symposium on High-level-language

Full text available:  pdf(740.42 KB)

Additional Information: full citation, abstract, references


Two results are presented in this paper: an enlargement of the concept of macro computers based on an inner machine oriented toward interpretation of machine languages; and a discussion of attributes of "directly interpretable languages"; and procedures for interpretation. "Sequential extraction" allows an instruction to be decoded; allows us to organize t ...

5 Affix grammar driven code generation

Mahadevan Ganapathi, Charles N. Fischer

October 1985

ACM Transactions on Programming Languages and Systems (TOP

Full text available:  pdf(3.19 MB)

Additional Information: full citation, abstract, references, citations

Affix grammars are used to describe the instruction set of a target architecture. A code generator is obtained automatically for a compiler using attributed parse trees. This model can automatically perform most popular machine-dependent optimizations. Code generators based on this model demonstrate retargetability for the VAX ...

6 A novel approach to character interfaces

Robert Cousins

March 1990

ACM SIGARCH Computer Architecture News, Volume 18 Issue 1

Full text available:  pdf(541.04 KB)

Additional Information: full citation, index terms

7 Verification of microprogrammed computer architectures in the S*-system:

W. Damm, G. Dohmen

December 1985 ACM SIGMICRO Newsletter , Proceedings of the 18th annual work:
Issue 4

Full text available:  pdf(1.43 MB)

Additional Information: full citation, abstract, referen

We apply the verification methodology underlying the S*-System[12], [13] to structured design [16] of an emulation of the instruction-set of a commercial available micro-architecture. Based on this case-study, we discuss some aspects of generation of microcode.

8 Computer-assisted instruction: Specification of attributes for CAI programs

Gloria M. Silvern, Leonard C. Silvern

January 1966

Proceedings of the 1966 21st national conference

Full text available:  pdf(1.15 MB)

Additional Information: full citation, abstract, references,

Man's search for knowledge began in antiquity and led ultimately to the invention of a book of 72 pages, was published in 1596. It contained spelling lessons and a short catechism. The first American textbook was published in 1641. This is the first press in the colonies, assembled only a few years before, in 1639. Nearly 200

9 Coding isomorphisms

William C. Lynch

February 1960

Communications of the ACM, Volume 3 Issue 2

Full text available:  pdf(263.22 KB)

Additional Information: full citation, abstract,

The coding of external symbols into symbols internal to a computer can sometimes preserve relevant informational properties, but in a form much more easily

10 Introducing computer concepts by simulating a simple computer

Robert A. Campbell

September 1996

ACM SIGCSE Bulletin, Volume 28 Issue 3

Full text available:  pdf(217.65 KB)

Additional Information: full citation, abstract, cit

The simulated computer consists of (1) main memory, (2) a register known as the CPU, and (4) an instruction counter. This computer recognizes 8 op codes (Add, Subtract, Multiply, Divide, Write, and Branch On Zero). The computer is simulated by creating a program that executes programs written by students, such as adding two numbers. The programs are written in machine language ...

11 BASICI—a simple computer to introduce computer organization and

Donald S. Miller, Bruce R. Millard

February 1982 Proceedings of the thirteenth SIGCSE technical symposium on Co

Full text available:  pdf(791.01 KB)

Additional Information: full citation, abstract,

BASICI is a simple interactive assembler-loader/interpreter which has been u: introductory course in computer organization and assembler language progr Department at Washington State University. Both “hardware” a emphasize basic concepts and to eliminate the confusion which occurs when i surrounded by the myriad of machine and assembler lan ...

12 An analysis of 8086 instruction set usage in MS DOS programs

T. L. Adams, R. E. Zimmerman

April 1989 ACM SIGARCH Computer Architecture News , Proceedings of the third i support for programming languages and operating systems, Volume 1

Full text available:  pdf(943.30 KB)

Additional Information: full citation, references, c

13 The Cornell program synthesizer: a syntax-directed programming environn

Tim Teitelbaum, Thomas Reps

September 1981

Communications of the ACM, Volume 24 Issue 9

Full text available:  pdf(1.12 MB)

Additional Information: full citation, abstract, references,

Programs are not text; they are hierarchical compositions of computational st and debugged in an environment that consistently acknowledges and reforc Synthesizer demands a structural perspective at all stages of program develo a common foundation: a grammar for the programming language. Its full-scr syntax-directed diagnostic interpreter c ...

Keywords: diagnostic interpreter, program development system, programmin syntax-directed editor, template

14 MICROSIM: A microinstruction simulator for teaching microprogramming a

Francis P. Mathur

October 1977

Proceedings of the 10th annual workshop on Microprogramm

Full text available:  pdf(753.43 KB)

Additional Information: full citation, abstract, refer

This paper describes in the format of a user's manual, along with an example and emulation. This program simulates at the microinstruction set level the a microprogram-controlled minicomputer. This simulator, as an instructional ve software engineering laboratory adjunct to a regular course in microprogramr

15 ABLE: A LISP-based layout modeling language with user-definable procedural design

Gary B. Goates, Suhas S. Patil

June 1981 Proceedings of the eighteenth design automation conference on Design Automation

Full text available:  pdf(692.32 KB)


Additional Information: full citation, abstract, references

ABLE, an array-based linguistic editor, is a layout modeling language for storing the LISP programming language. This paper describes ABLE's design, present ABLE's usefulness in SLA-based circuit design. ABLE embodies a linguistic approach to very large scale integrated (VLSI) circuits; digital system designers can represent relatively abstract and hierarchical designs in a more intuitive manner.

16 Modeling and control of robotic mine haulage system

Ernest G. Holzmann, Kenneth B. Haefner

March 1982 Proceedings of the fifteenth annual simulation symposium

Full text available:  pdf(1.03 MB)

Additional Information: full citation, abstract, references

Concepts borrowed from discrete and hybrid system simulation have been successfully applied to a complex, distributed computer control system. The example presented is a robotic mine. The system controls all train movements and haulage operations into a single embedded in the system software, distributed over three levels: 1. Central control, 2. Wayside control, 3. Train control.

17 Address size independence in a 16-bit minicomputer

Philip E. Stanley

April 1978 Proceedings of the 5th annual symposium on Computer architecture

Full text available:  pdf(648.93 KB)

Additional Information: full citation, abstract, references

Most minicomputers do not distinguish in their architecture between address and operand size. Address size becomes a de facto limit on address size (and thus memory size) in many architectures when attempting to build systems with large address space. This paper describes a "transparent" architecture to the programmer and independent of operand size.

18 Retargetable Compiler Code Generation

Mahadevan Ganapathi, Charles N. Fischer, John L. Hennessy


December 1982 ACM Computing Surveys (CSUR), Volume 14 Issue 4

Full text available:  pdf(1.93 MB) Additional Information: full citation, references, citations, index terms

19 The contribution to performance of instruction set usage in System/370

O. R. LaMaire, W. W. White

November 1999 Proceedings of 1986 fall joint computer conference on Fall joint computer conference

Full text available:  pdf(1.18 MB)

Additional Information: full citation, references, citations, index terms

20 A verification technique for gated clock

Masamichi Kawarabayashi, Narendra Shenoy, Alberto Sangiovanni-Vincentelli

July 1993 Proceedings of the 30th international on Design automation conference




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21 The George Washington University Core System implementation

James D. Foley, Patricia A. Wenner

August 1981

Proceedings of the 8th annual conference on Computer graphics and graphics systems

Full text available: pdf(728.20 KB)

Additional Information: full citation, abstract, reference

A full implementation of the proposed standard Core System graphics subrou described. Emphasis is placed on the internal structure of the implementation features of the implementation include separate 2D and 3D viewing pipelines flow of information between various parts of the Core, a strong separation be device-dependent parts of t ...

22 Storage concepts in a software-reliability-directed computer architecture

Glenford J. Myers

April 1978

Proceedings of the 5th annual symposium on Computer architecture and computer systems

Full text available: pdf(513.49 KB)

Additional Information: full citation, abstract, reference

Because of the tremendous difficulty of producing reliable software (applicati consequences of software errors, a new solution is being explored: the develc will substantially enhance the reliability of the programs executing above it. concepts (e.g., data representations and addressing) in the architecture.

23 Graphics language / one - IBM Corporate-Wide physical design data format

David R. Lambert

June 1981 Proceedings of the eighteenth design automation conference on Design Automation

Full text available:  pdf(392.15 KB)

Additional Information: full citation, abstract, references

The evolution and structure of the IBM Corporate-Wide physical design data format is discussed. The need for a common graphics interface for communication architecture is demonstrated. At IBM, the same format is used from physical layout to mask printed circuit board designs.

24 Packed scatter tables

Gordon Lyon

October 1978

Communications of the ACM, Volume 21 Issue 10

Full text available:  pdf(834.68 KB)

Additional Information: full citation, abstract, references

Scatter tables for open addressing benefit from recursive entry displacements and auxiliary cost functions. Compared with conventional methods, the new technique that resemble exact-solution optimal packings. The displacements are depth-(exhaustive) optimization, although packing costs remain linear— $O(n)$.
Keywords: assignment problem, backtrack programming, hashing, open address rearrangements

25 The basic side of tape labeling

William A. Logan

February 1960

Communications of the ACM, Volume 3 Issue 2

Full text available:  pdf(214.14 KB)


Additional Information: full citation, abstract, references

Once an installation has determined that it would be advantageous to be able to read a reel of tape on hand and to be able to check those identifications by program Labeling Routine. The parameters of such a routine are limited only by the installation as they request (and frequently demand) that the label on the tape tallies, messages, remain ...

26 Optimizing direct threaded code by selective inlining

Ian Piumarta, Fabio Riccardi

May 1998 ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1998 conference
implementation, Volume 33 Issue 5

Full text available:  pdf(1.28 MB)

Additional Information: full citation, abstract,


Achieving good performance in bytecoded language interpreters is difficult with portability. This is due to the complexity of dynamic translation ("just-in-time code, which is the mechanism employed universally by high-performance interpreters). Techniques make it possible to create highly-portable dynamic translators that have the performance of optimized C for certain cases ...

Keywords: bytecode interpretation, dynamic translation, inlining, just-in-time

27 Simulation structure for the development of Texas Instruments' Advanced :

Sidney D. Nolte, Marvin T. Talbott

June 1973 Proceedings of the 1973 symposium on Simulation of computer systems

Full text available:  pdf(1.10 MB)

Additional Information: full citation, abstract, references

During development of a large-scale computer system, design decisions must be based on experience. As development continues past the design phase, it is necessary to ensure that the subsystem is doing what it was designed to do from both functional and performance points of view. It is necessary to have some means of evaluating the effects of proposed changes in the design tool in satisfying ...

28 The implementation of a user-extensible system on a dynamically microprogrammable

Fergus K. Fung, Willis K. King

October 1977 Proceedings of the 10th annual workshop on Microprogramming

Full text available:  pdf(308.59 KB)

Additional Information: full citation, abstract, references

On a dynamically user-microprogrammable computer the user can tailor the system by adding microprogrammed routines and adding them to the system. If these routines are added using them is no different from using any other basic machine instruction of the system. The design and implementation of such a user-extensible system is described in a paper which manages a virtual memory for ...

29 Contemporary Concepts of Microprogramming and Emulation

Robert F. Rosin


December 1969 ACM Computing Surveys (CSUR), Volume 1 Issue 4

Full text available:  pdf(1.40 MB) Additional Information: full citation, references, citations, index terms

30 Hardware and software support for efficient exception handling

Chandramohan A. Thekkath, Henry M. Levy

November 1994 Proceedings of the sixth international conference on Architectural operating systems, Volume 29 , 28 Issue 11 , 5

Full text available:  pdf(1.44 MB)


Additional Information: full citation, abstract, references

Program-synchronous exceptions, for example, breakpoints, watchpoints, illegal instructions, provide information about exceptional conditions, interrupting the program at a handler. Over the last decade, however, programs and run-time systems have used exceptions as a performance optimization to detect normal and expected conditions. Unfortunately,

31 An architectural framework for migration from CISC to higher performance

Gabriel M. Silberman, Kemal Ebcioglu

August 1992 Proceedings of the 6th international conference on Supercomputing

Full text available:  pdf(2.04 MB)

Additional Information: full citation, abstract, references,

We describe a novel architectural framework that allows software applications to migrate from Set Computer (CISC) to a different, higher performance architecture without the intervention of the application user or developer. The framework provides a hardware mechanism for migrating between two instruction sets, resulting in a machine that enhances application program behavior (from a user perspective ...)

32 Hardware combining and scalability

Susan R. Dickey, Richard Kenner

June 1992 Proceedings of the fourth annual ACM symposium on Parallel algorithms and architectures

Full text available:  pdf(967.92 KB)

Additional Information: full citation, references, citations, index

33 META II a syntax-oriented compiler writing language

D. V. Schorre

January 1964

Proceedings of the 1964 19th ACM national conference

Full text available:  pdf(782.31 KB)

Additional Information: full citation, abstract, references

META II is a compiler writing language which consists of syntax equations representing instructions to output assembly language commands are inserted. Compared to VALGOL I and VALGOL II. The former is a simple algebraic language design. The latter contains a fairly large subset of ALGOL 60. The method of writing a compiler paper may be explained ...

34 A MULTILINGUAL INTERPRETER for interactive computing in an academ

Larry Kheriaty

August 1973

Proceedings of the annual conference

Full text available:  pdf(381.53 KB)

Additional Information: full citation, abstract

In order to satisfy three types of terminal users, student programmers, production programmers, and researchers, Washington State College has developed a MULTILINGUAL INTERPRETER. The interpreter supports BASIC and COURSEWRITER III to be run on a single terminal system. The compiler is such that programs can be prepared in more than one source language. The interpreter provides advanced programming features not only ...

35 A microcoded real-time executive for numeric support nodes distributed with

J. O. Bondi

January 1988

Proceedings of the 21st annual workshop on Microprogramming and

Full text available:  pdf(305.46 KB)


Additional Information: full citation, abstract, references

The mix of nodes within heterogeneous embedded networks typically includes: oriented nodes particularly adept at efficient manipulation of regularly structured data; "Array Processing" (AP) nodes usually serve other more general control of each AP is maintained by a microcoded AP-resident executive program and tuned to minimize ...

36 Enabling trusted software integrity

Darko Kirovski, Milenko Drinić, Miodrag Potkonjak

October 2002

Tenth international conference on architectural support for program
Proceedings of the 10th international conference on architectural support for
operating systems (ASPLOS-X), Volume 37, 30, 36 Issue 10, 5,Full text available:  pdf(1.39 MB)

Additional Information: full citation, abstract

Preventing execution of unauthorized software on a given computer plays a problem is that although a program at the beginning of its execution can be redirected to externally injected malicious code using, Existing techniques address this problem by trying to detect the intrusion at software is not prone to a problem ...

37 Description-driven code generation using attribute grammars

Mahadevan Ganapathi, Charles N. Fischer

January 1982

Proceedings of the 9th ACM SIGPLAN-SIGACT symposium on Principles of

Full text available:  pdf(988.59 KB)

Additional Information: full citation, abstract

The instruction-set of a target architecture is represented as a set of attributes obtained automatically for any compiler using attributed parsing techniques. The compiler automatically perform most popular machine-dependent optimizations, including a code generator is also easily retargetable to different machine architectures.

38 High-level power estimation (invited talks): A multi-level strategy for softwa

C. Brandolese, W. Fornaciari, L. Pomante, F. Salice, D. Sciuto

September 2000

Proceedings of the 13th international symposium on Syster

Full text available:  pdf(117.56 KB)

Additional Information: full citati

In this paper a comprehensive methodology for software power estimation is by rigorous mathematical models of power consumption at three different lev been validated in a complete framework developed within the TOSCA co-desi

39 An example RISC vector machine architecture

Martin Dowd

September 1987 ACM SIGARCH Computer Architecture News, Volume 15 Issue 4


Full text available:  pdf(484.57 KB)

Additional Information: full citation, index terms

40 Interleaving: a multithreading technique targeting multiprocessors and work

James Laudon, Anoop Gupta, Mark Horowitz

November 1994 Proceedings of the sixth international conference on Architectural operating systems, Volume 29 , 28 Issue 11 , 5

Full text available:  pdf(1.35 MB)

Additional Information: full citation, abstract, references

There is an increasing trend to use commodity microprocessors as the compu However, given that the majority of the microprocessors are sold in the work market, it is only natural that architectural features that benefit only multipr commodity microprocessors. In this paper, we explore multiple-context proce to hide the large me ...

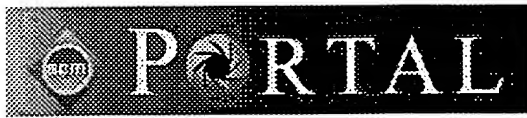
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41 Design tradeoffs for software-managed TLBs

Richard Uhlig, David Nagle, Tim Stanley, Trevor Mudge, Stuart Sechrest, Richard Uhlig
August 1994 ACM Transactions on Computer Systems (TOCS), Volume 12 I

Full text available: pdf(1.85 MB)

Additional Information: full citation, abstract, references, citations

An increasing number of architectures provide virtual memory support through software management can impose considerable penalties that are highly dependent on its use of virtual memory. This work explores software-managed TLB design across a range of monolithic and microkernel operating systems. Through hardware monitoring, we measure performance for benchmarks running on a ...

Keywords: hardware monitoring, translation lookaside buffer (TLB), trap-driven

42 Delta storage for arbitrary non-text files

Christoph Reichenberger
May 1991 Proceedings of the 3rd international workshop on Software configuration management

Full text available: pdf(634.58 KB)



Additional Information: full citation, references, citations, index terms

43 An Efficient Compiler Technique for Code Size Reduction Using Reduced I

A. Halambi, A. Shrivastava, P. Biswas, N. Dutt, A. Nicolau

March 2002

Proceedings of the conference on Design, automation and test in

Full text available:  pdf(289.61 KB)  Publisher Site

Additional Info

For many embedded applications, program code size is a critical design factor. size is to employ a "dual instruction set", where processor architectures support and a narrow, space-efficient (usually 16 bit) Instruction Set with a limited set of registers. This feature, however, requires compilers that can reduce code size. Existing compiler ...

44 An advanced tactical computer concept

Kenneth J. Thurber, Peter C. Patton, Robert C. Deward, Jon C. Strauss, Thomas

March 1977 ACM SIGARCH Computer Architecture News, Proceedings of the 4th : architecture, Volume 5 Issue 7

Full text available:  pdf(432.42 KB)

Additional Information: full citation, abstract, refer

This paper discusses the design of a real-time computer. The computer's design architecture are summarized. The paper discusses how the design requirements. The system's three upward compatible addressing options (real, base, virtual

45 Micro emulation: When to do it and when not to do it

Lee Hoevel

September 1973

Conference record of the 6th annual workshop on Micropro

Full text available:  pdf(723.79 KB)

Additional Information: full citation, abstract, refer

In this paper, we will attempt to analyze those conditions under which the use of the performance of a two-phase processing system. This analysis is couched in terms of "ideal" DEL, given a particular source language SL and base machine. The system would minimize the overall space and time needed to evaluate a typical SL program.

46 Teaching basic computer organization through "microprogramming"

Miriam R. Tausner





September 1973

Conference record of the 6th annual workshop on Micropro

Full text available:  pdf(170.19 KB)

Additional Information: full citation, abstract, citi

To reinforce concepts of CPU organization students are asked to write a program to be run on a theoretical microprogrammable computer which is simulated using

- 47 Direct microprogrammed execution of the intermediate text from a high-level language**
Francois Robert Broca, Richard E. Merwin
May 1973 Proceedings of the meeting on SIGPLAN/SIGMICRO interface
Full text available:  pdf(654.98 KB) Additional Information: full citation, abstract, references
- Microprogramming commonly executed operations can improve the computation of a high-level language compiler after syntactic and semantic analysis of the input text. This paper describes how microprogramming may be used to execute directly high-level language compiler after syntactic and semantic analysis of the input text. The microprogrammed execution of common forms of intermediate text - i.e.: quadruples, is simulated. A comparison is made, in terms of storage and execution time, between the microprogrammed execution and the conventional execution.
- 48 Representation: Out-of-core encoding of large tetrahedral meshes**
Shyh-Kuang Ueng
July 2003 Proceedings of the 2003 Eurographics/IEEE TVCG Workshop on Volume Rendering
Full text available:  pdf(210.67 KB) Additional Information: full citation, abstract, references
- In this paper, an out-of-core data compression method is presented to encode large tetrahedral meshes. The method is comprised with two stages. At the first stage, the input meshes are divided into octants, based on an octree structure. Each octant must contain less than 256 FEA cells. The octants are then traversed to enumerate the cells and store them into the main memory. Octants produced in the data division are stored in disk. The octants are then traversed to enumerate the cells and store them into the main memory.
- 49 Direct microprogrammed execution of the intermediate text from a high-level language**
Francois Robert Broca, Richard E. Merwin
August 1973 Proceedings of the annual conference
Full text available:  pdf(521.76 KB) Additional Information: full citation, abstract, references
- Microprogramming commonly executed operations can improve the computation of a high-level language compiler after syntactic and semantic analysis of the input text. This paper describes how microprogramming may be used to execute directly high-level language compiler after syntactic and semantic analysis of the input text. The microprogrammed execution of common forms of intermediate text - i.e.: quadruples, is simulated. A comparison is made, in terms of storage and execution time, between the microprogrammed execution and the conventional execution.
- 50 Languages for direct execution**
Lee W. Hoevel
September 1974 Conference record of the 7th annual workshop on Microprogramming
Full text available:  pdf(775.94 KB) Additional Information: full citation, abstract, references
- The utility of a modern computing system lies in its capacity to perform a variety of operations under user control. In the earliest systems users exerted direct, low-level control, in which a user applied to a data item manually at the time it was to be performed. In the early 1960s, the user controls a small electronic calculator. With the passage of time, this user control has become more sophisticated, culminating in the development of modern computing systems.

51 Micro control hardware and high level languages interpreter: An attempt of

J. Demarteau

September 1974

Conference record of the 7th annual workshop on Micropro

Full text available:  pdf(512.38 KB)

Additional Information: full citation, abstract, refer

The aim of this paper is to try and describe a new technique for implementing interpreter of macro-languages. It demonstrates the connexion between the micro-instruction and the structure of a dynamic interpreter. The proposed micro-fetch/generator instruction (1), is founded on a microprocedure call generator. The CPU are split into two specific levels : t ...

Keywords: Address control, Architecture, Instruction-generator, Macro-genera

52 A logical approach to teach digital computer design at logic and systems le

Sarma R. Vishnubhotla

February 1977

Proceedings of the seventh SIGCSE technical symposium on Con

Full text available:  pdf(473.90 KB)

Additional Information: full citation, abstra

Design courses in Computer Systems Design are being taught in many under Science and Electrical Engineering students. A design project is explained in 1 students regarding the important concepts in both logic and systems level. TI memory and a single index register. This project can also be enlarged by intr

53 MBALM/1700: A microprogrammed LISP machine for the Burroughs B1720

M. L. Griss, M. R. Swanson

October 1977

Proceedings of the 10th annual workshop on Microprogramm

Full text available:  pdf(1.02 MB)

Additional Information: full citation, abstract, references,

This paper describes the implementation of BALM and LISP processors for the processors consist of an interpreter of MBALM pseudo-code (written in MIL), a code (written in BALM or LISP). Of particular interest is the modular design o to evaluate and improve the size and speed of the machine. The current syst compilation, compacting garbag ...

54 Evolution in the design of abstract machines for software portability

Daniel Thalmann

May 1978

Proceedings of the 3rd international conference on Software engin

Full text available:  pdf(535.40 KB)

Additional Information: full citation, abstract, reference

The abstract machine model is the best one for solving the difficult problem c the design of these machines is necessary. After a brief survey of the well-kn the design of a more general one to implement portable operating systems. T abstract machine to existing computers is discussed and the paper explains h inestimable means to reduce the ...

55 Design of a Lisp machine - FLATS

E. Goto, T. Soma, N. Inada, T. Ida, M. Idesawa, K. Hiraki, M. Suzuki, K. Shimizu
August 1982 Proceedings of the 1982 ACM symposium on LISP and functional

Full text available:  pdf(501.49 KB)

Additional Information: full citation, abstract, reference:

Design of a 10 MIPS Lisp machine used for symbolic algebra is presented. By mechanisms which greatly speed up primitive Lisp operations, the machine is for content addressed associative tabulation and a very fast multiplier for speed fast hash address generation.

56 Compiler chip: A hardware implementation of compiler

Akira Fusaoka, Masaharu Hirayama

March 1982 Proceedings of the first international symposium on Architectural support for operating systems

Full text available:  pdf(301.61 KB)

Additional Information: full citation, abstract, reference:

In this paper we discuss about another approach: Compiler Chip, which is a VLSI chip. Constructing a compiler by a few VLSI chip, the computer manufacturer can use these chips are installed in a intelligent terminal in order to remove the compiler from the mainframe.

57 An experiment to improve operand addressing

Robert P. Cook, Nitin Donde

March 1982 Proceedings of the first international symposium on Architectural support for operating systems

Full text available:  pdf(398.18 KB)

Additional Information: full citation, abstract, reference:

MCODE is a high-level language, stack machine designed to support strongly typed variety of data types in a modular programming environment. The instruction set extensibility, is based on an analysis of 120,000 lines of Pascal programs. The instruction sets of the Digital Equipment PDP-11 and VAX by examining them for all three machines. In addition ...

Keywords: Addressing modes, Computer architecture, Stack machine

58 A Metafile for efficient sequential and random display of graphics

Theodore N. Reed

July 1982 Proceedings of the 9th annual conference on Computer graphics and

Full text available:  pdf(386.23 KB)

Additional Information: full citation, abstract, refer

Graphics metafiles have been in use at the Los Alamos National Laboratory since it was defined in 1976 and has been updated several times to allow efficient graphics environment. History and current applications of the Common Graphics System, its objectives, details of the format, and random access extensions incorporated

Keywords: Device-independent, Metafile, Random access

59 Computer-1—a modern simple computer to introduce computer organization and programming

Donald S. Miller

February 1983 Proceedings of the fourteenth SIGCSE technical symposium on Computer science education

Full text available:  pdf(537.52 KB)

Additional Information: full citation, abstract, reference

COMPUTER-1 is an interactive editor/assembler simulator-debugger and program development instructional tool for an introductory course in computer organization and assembly language. COMPUTER-1's organization, assembler language and interactive facilities are designed to teach computer architecture and assembly language programming while minimizing the dependent details present during this learning period. COMPUTER-1 ...

60 Structured design verification: Function and timing

C. J. Rimkus, M. R. Wayne, D. D. Cheng, F. J. Magistro

June 1983 Proceedings of the twentieth design automation conference on Design automation

Full text available:  pdf(569.17 KB)

Additional Information: full citation, abstract, reference




Changes in the design verification environment brought about by VLSI design technology modelling support is now required of efficient, interactive verification tools. This environment is analyzed, especially in early error removal during the design process. It has been implemented as part of the IBM Design and Verification system, is described, and the key areas of his ...

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Circuits and Systems, 2000. IEEE APCCAS 2000. The 2000 IEEE Asia-Pacific Conference on , 4-6 Dec. 2000

Page(s): 485 -488

[\[Abstract\]](#) [\[PDF Full-Text \(296 KB\)\]](#) **IEEE CNF****2 Near fine grain parallel processing of circuit simulation using direct method***Maekawa, Y.; Nakano, K.; Takai, M.; Kasahara, H.;*

Communications, Computers, and Signal Processing, 1995. Proceedings. IEEE Pacific Rim Conference on , 17-19 May 1995

Page(s): 272 -276

[\[Abstract\]](#) [\[PDF Full-Text \(396 KB\)\]](#) **IEEE CNF****3 Gate array or microcontroller? The engineers dilemma. A 4-bit microcontroller replacement case study***Mulroy, T.J.;*

Microprocessor or ASIC - Choice and Implementation, IEEE Colloquium on , 21 Dec 1995

Page(s): 2/1 -2/2

[\[Abstract\]](#) [\[PDF Full-Text \(84 KB\)\]](#) **IEEE CNF****4 Code generation for the AT&T DSP32***Baudendistel, K.; McClellan, J.H.;*

Acoustics, Speech, and Signal Processing, 1990. ICASSP-90., 1990 International Conference on

Conference on , 3-6 April 1990

Page(s): 1073 -1076 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(344 KB\)\]](#) **IEEE CNF**

5 HW/SW codesign for embedded telecom systems

Antoniuzzi, S.; Balboni, A.; Fornaciari, W.; Sciuto, D.;

Computer Design: VLSI in Computers and Processors, 1994. ICCD '94. Proceedings
IEEE International Conference on , 10-12 Oct. 1994

Page(s): 278 -281

[\[Abstract\]](#) [\[PDF Full-Text \(384 KB\)\]](#) **IEEE CNF**

6 A methodology for control-dominated systems codesign

Antoniuzzi, S.; Balboni, A.; Fornaciari, W.; Sciuto, D.;

Hardware/Software Codesign, 1994., Proceedings of the Third International Wo
on , 22-24 Sept. 1994

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[\[Abstract\]](#) [\[PDF Full-Text \(652 KB\)\]](#) **IEEE CNF**

7 A unified scheduling model for high-level synthesis and code generati

Kifli, A.; Goossens, G.; De Man, H.;

European Design and Test Conference, 1995. ED&TC 1995, Proceedings. , 6-9 M
1995

Page(s): 234 -238

[\[Abstract\]](#) [\[PDF Full-Text \(500 KB\)\]](#) **IEEE CNF**

8 Constraint driven code selection for fixed-point DSPs

Bashford, S.; Leupers, R.;

Design Automation Conference, 1999. Proceedings. 36th , 21-25 June 1999

Page(s): 817 -822

[\[Abstract\]](#) [\[PDF Full-Text \(580 KB\)\]](#) **IEEE CNF**

9 Automated design of custom femoral stem prosthesis

Mandala, A.K.;

Bioengineering Conference, 1991., Proceedings of the 1991 IEEE Seventeenth A
Northeast , 4-5 April 1991

Page(s): 56 -59

[\[Abstract\]](#) [\[PDF Full-Text \(180 KB\)\]](#) **IEEE CNF**

10 A simulator for general purpose optical arrays

Marvin, W.B.; Burleson, W.P.;

Computer Design: VLSI in Computers and Processors, 1991. ICCD '91. Proceedings
1991 IEEE International Conference on , 14-16 Oct. 1991

Page(s): 486 -489

[\[Abstract\]](#) [\[PDF Full-Text \(388 KB\)\]](#) **IEEE CNF**

11 Critical performance path analysis, and efficient code generation in the Seamless architecture

*Bright, D.L.; Fineberg, S.A.; Pease, B.H.; Roderick, M.L.; Sundaram, S.; Casava
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